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HIGH RESOLUTION TIME-INTERVAL MEASUREMENT SYSTEMS APPLIED TO FLOW MEASUREMENT

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Abstract

The designing process of high resolution time interval measurement systems creates many problems that need to be eliminated. The problems are: the latch error, the nonlinearity conversion, the different duty cycle coefficient of the clock signal, and the clock signal jitter. Factors listed above affect the result of measurement. The FPGA (Field Programmable Gate Array) structure also imposes some restrictions, especially when a tapped delay line is constructed. The article describes the high resolution time-to-digital converter, implemented in a FPGA structure, and the types of errors that appear there. The method of minimization and processing of data to reduce the influence of errors on the measurement is also described.

Keywords: FPGA, time-to-digital converter, multi-segment delay line, carry chain.

1. Introduction

The Time Interval Measurement System (TIMS) has many applications. TIMS may be used e.g.: in laser rangefinders, in ultrasonic flowmeters in time of flight mass spectrometers, in systems to luminescence decay measurement, or in telecommunications, when cable damage is localized.

Fundamental metrological parameters of the TIMS are: the range of measurement, resolution, dead time and power consumption. These parameters are strongly dependent on time interval measurement methods and FPGA structure technology which has been applied. Among time interval measurements such methods can be pointed out: time-stretching, direct time to digital conversion (a tapped delay line), a Vernier time to digital converter or, the simplest of them, a simple counter [1-5]. In general, the Time to Digital Converter (TDC) is implemented in programmable structures FPGA or CPLD and ASIC. Of course, better system performance is obtained by using ASICs [6, 7] than FPGAs, but for a prototype small series of FPGA structures are used. This is done because one can easily modify the system and its operation at the designing process. However, implementation in the FPGA programmable structure, which has its own limitation, of a Tapped Delay Line (TDL) is not a simple task, as well as obtaining low power consumption.

This article describes in detail the high resolution system implemented in a FPGA structure. Moreover the main sources of the conversion errors and methods of their minimization are also described.

The first part describes the construction of the system and the principle of time to digital conversion. The next chapter describes in detail the sources of error, such as clock distribution, error of count of reference clock periods, delay fluctuations and reference signal imperfections. The designed system is applied to measure flow rate. Afterwards some results

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of the flow measurement and the conversion characteristics will be shown. The final section provides a summary.

2. Construction of high resolution measuring system

The whole system is implemented in a programmable FPGA Virtex 5 device. The block diagram of TIMM is presented in Fig. 1. The TIMM consists of TDL with registers, clock counters, memory blocks and interface.

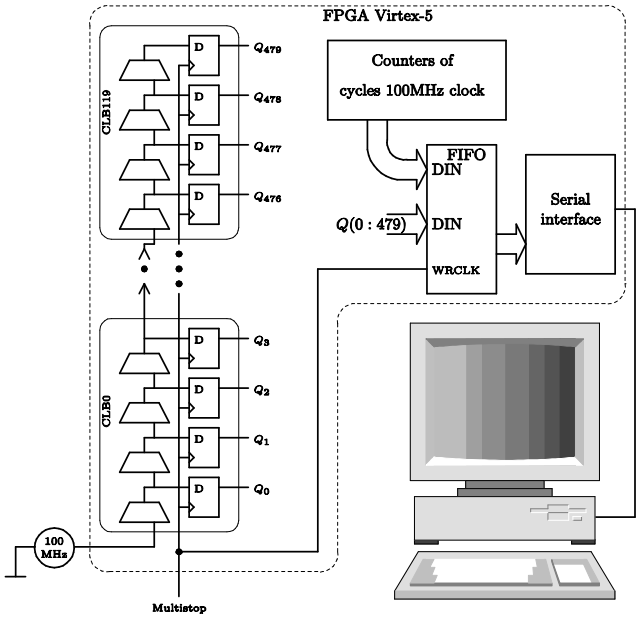

Fig. 1. Time interval measurement system based on a FPGA structure.

The fundamental element of the high resolution time interval measurement module (TIMM) is the TDL. Single block delay in TDL is obtained using the carry chain elements. Usually these elements are used to realize an arithmetic function.

Using the carry chain for the delay elements implementation, an average resolution of approximately $q = 15\,ps$ can be obtained. The characteristics of the TIMM is shown in Fig. 2.

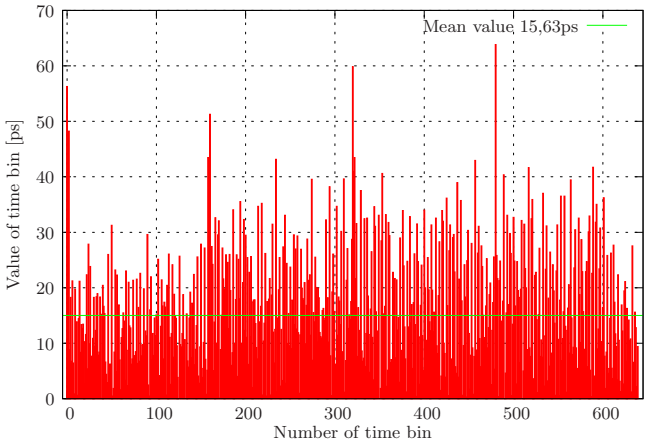

Fig. 2. The delay value of each segment of the TIMM delay line.

A test of density code is used to create this characteristics.

The reference signal from a quartz oscillator is applied to the first segment of TDL. The number of delay elements is selected to cover the entire period of the reference signal.

Metrol. Meas. Syst., Vol. XXI (2014), No. 1, pp. 77–84.

In this case the TDL is built of four hundred and eighty elements. Each of the delay elements with register is associated. The register data input (D-type flip-flop) is connected directly with the carry chain, but the clock input is fed to a global "Start/Multistop" input. This allows to properly distribute input pulses in the programmable structure.

At each rising edge on "Start/Multistop" input the data from TDL registers and clock counters is stored in a FIFO memory. The data in the form of time stamps is composed of two parts. One of them, as described earlier, is taken from TDL registers, while the other is taken from the clock counter.

Generally, the clock counters could be read when they are incremented. It is a source of time interval measurement errors. Therefore, the system has two counters working alternately. The first of them works at the rising edge of the clock signal, while the second works at the falling edge of the clock signal. The choice of counters is performed by using a multiplexer controlled by the phase value.

The data (time stamps) stored in memory blocks of FPGA is sent later to the computer after the end of each measuring cycle. Only a single programmable FPGA structure was used. It was the XC5VLX50-1FF676, where about 3 percent of Slice Registers, about 4 percent of Slice LUTs, about 33 percent of BlockRAM were used.

3. Principle of time interval measurement

The main task of the measuring system is to register the time stamps corresponding to input pulses fed to the "Start/Multistop" input. The principle of operation of the measurement system is shown in Fig. 3.

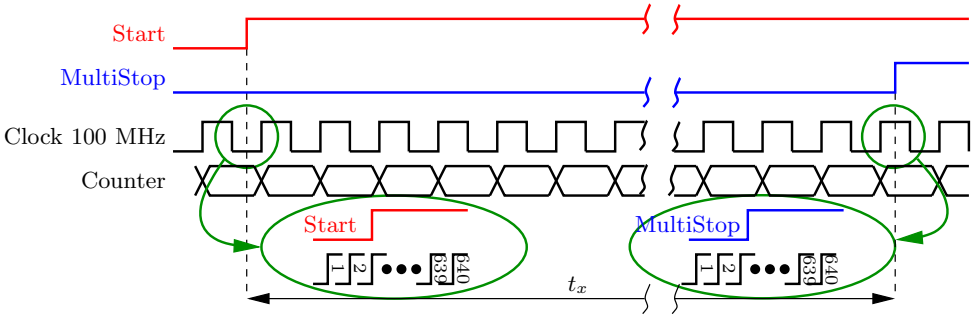

Fig. 3. Diagram showing the principle of time interval measurement.

TIMM has an input circuit, where the logical sum of signals from the "Start" input and the "Multistop" input is created. The "Start" input has a higher priority than the "Multistop" input, therefore the "Multistop" input is locked by it. In this way the beginning of the time interval measurement is defined precisely. The time interval measured by TIMM can be described as:

$$t_x = N \cdot T + p_i \cdot \overline{\tau} + p_j \cdot \overline{\tau}, \tag{1}$$

where: N – the number of clock signal pulses registered by the counter; T – period of the reference clock; p_i, p_j – the TDL registers value for "Start" and "Multistop" pulses respectively; $\overline{\tau}$ – the mean value of channel width.

Using this equation, it should be noted that the precision of time interval measurement depends on: the precision of the interpolator (TDL) and jitter of the reference clock. The interpolator characteristic is shown in Fig. 2. The average value of single delay element is about 15 ps.

By subtracting the time bin width of the i-th channel from the average value, differential nonlinearity can be calculated as:

$$DNL_i = \tau_i - \overline{\tau}. \tag{2}$$

Summing up the particular deviation from the average channel width, integral nonlinearity errors will be given as:

$$INL_i = \sum_{i=0}^{M-1} \left(\tau_i - \overline{\tau}\right). \tag{3}$$

The integral nonlinearity error determines how large an error during the measurement of a time-interval, using this module, will be committed.

Therefore, the more accurate time interval measurement method is summing successively time bins as it is shown below:

$$t_x = N \cdot T + \sum_{i=0}^{p_i} \tau_i - \sum_{j=0}^{p_j} \tau_j, \tag{4}$$

where: τ_i, τ_j – are the real time bin widths.

In this way, the influence of integral nonlinearity is minimized.

4. Error sources and their minimization

The main sources of errors in the TIMM are for example: TDL nonlinearity error which also follows the construction of the programmable FPGA structure, counter errors, single element of TDL delay fluctuations, metastability and reference clock signal stability.

As it has been shown earlier, the time interval measurement uncertainty associated with the time to digital converter (TDC) depends on the measurement method. As a result of measurement an N – elements vector is obtained. This vector describes the reference clock phase. This information should be written in the thermometer code. If the information consists of logical '0' and '1' uninterruptedly ("...0000011111..."), then it is the correct value. In most cases, this sequence is disordered ("...0011011011..."). This may indicate that there are time differences between flip-flop clock inputs.

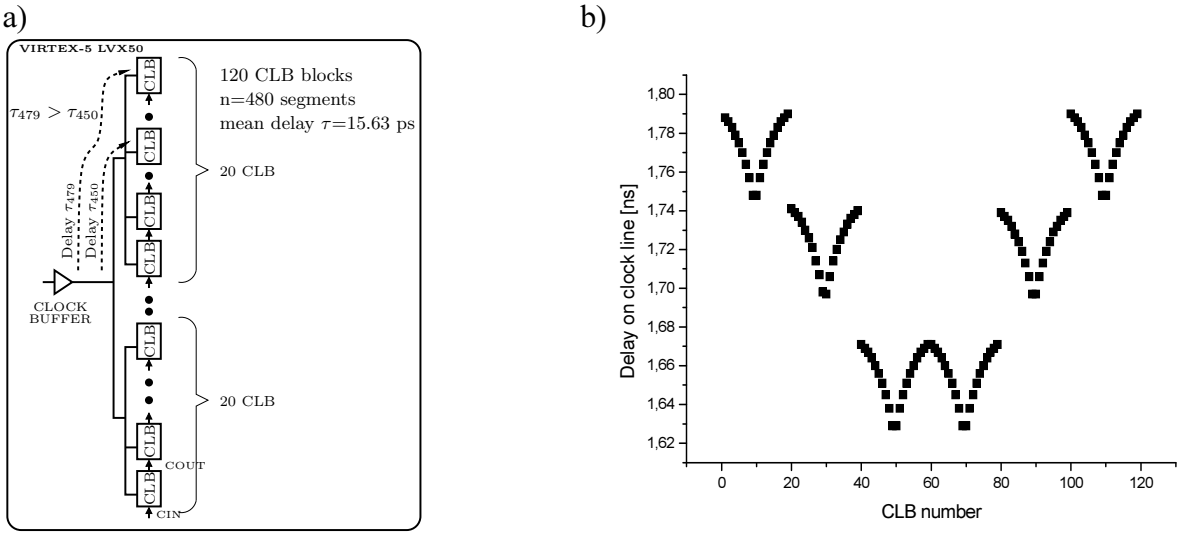

Fig. 4. Signal distribution in the FPGA structure: a) construction of TDL, b) delay between the clock buffer and configurable logic block (CLB).

Metrol. Meas. Syst., Vol. XXI (2014), No. 1, pp. 77–84.

The Figure 4b shows the delay between the clock buffer output and the CLB's input. This result is obtained from a model of the FPGA structure [8]. There are visible discontinuities for CLB numbers 20th, 40th, 80th and 100th. This is caused by the technology of signal distribution where the signal is divided into smaller regions. This creates errors in TDL registers and the result in the thermometer code cannot be obtained.

This problem was solved by changing the sequence of TDL register bits.

Because the time stamps are composed of two parts, the next error source of TIMM is a counter. Large errors occur when its value is incremented when the data is transferred to FIFO memory [5]. The system is protected from such errors by using two independent counters and the multiplexer (Fig. 5).

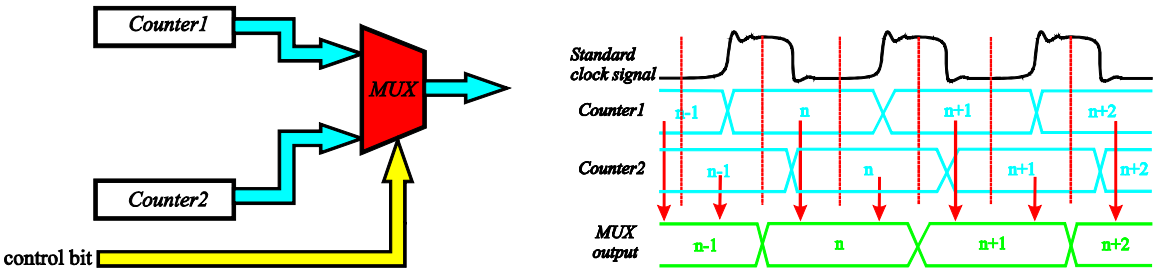

Fig. 5. Counter error protection a) block diagram, b) timing diagram.

This solution is quite effective.

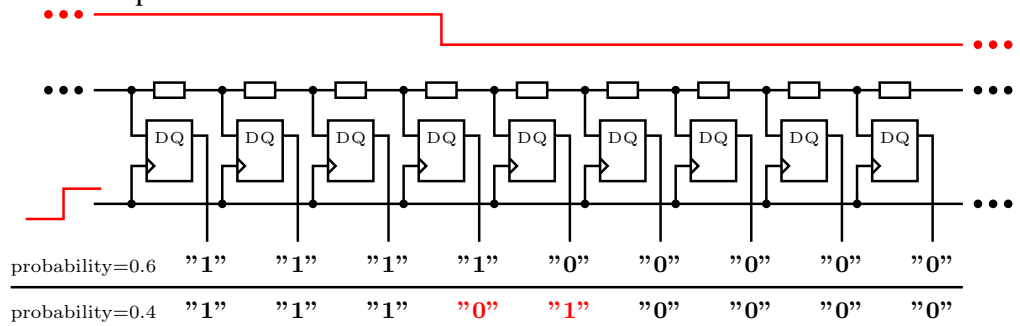

Fig. 6 Single element of TDL delay fluctuation.

Another type of error in TIMM is a single element of TDL delay fluctuation. Similarly to the case where the nonlinearity error dependent on construction of the programmable structure was described, here also the result is not written in the thermometer code. This can be seen when, for example, a wrong vector value "...00101111..." is randomly received instead of the expected "...00001111..." (Fig. 6). It may be explained as delay fluctuations of a single TDL element or the various parameters of neighboring flip-flops. There are two ways to eliminate this phenomenon: hardware and software. If the hardware method is used, then a special algorithm must be implemented. This algorithm in VHDL is presented below:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity correct is
    Port ( we            : in std_logic_vector(479 downto 0);
           wy            : out std_logic_vector(479 downto 0)
         );
end correct;
```

```
architecture correct of correct is
begin
  wy(wy'low) <= we(we'low) or (we(we'low+1)and (not we(we'low+2)));
  wy(wy'low+1) <= (we(we'low) and we(we'low+2)) or (we(we'low+1) and we(we'low+2)) or
(we(we'low) and we(we'low+1));
  corr: for i in wy'low+2 to wy'high-2 generate
     wy(i) <= ((we(i) and we(i-1) and we(i-2))or (we(i+1) and we(i-1) and we(i-2))or
(we(i+1) and we(i) and we(i-2))or
                                  (we(i+1) and we(i) and we(i-1))or (we(i+2) and we(i-1)
and we(i-2))or (we(i+2) and we(i) and we(i-2))or
                                  (we(i+2) and we(i) and we(i-1))or (we(i+2) and we(i+1)
and we(i-2))or (we(i+2) and we(i+1) and we(i-1))or
                                  (we(i+2) and we(i+1) and we(i)));
  end generate;
  wy(wy'high-1) <= we(we'high-2) or (we(we'high-1)and (not we(we'high)));
  wy(wy'high) <= (we(we'high-2) and we(we'high)) or (we(we'high-1) and we(we'high)) or
(we(we'high-2) and we(we'high-1));

end correct;
```

The data thus obtained is stored in a FIFO memory and then it is sent to the computer. In the software case the data from TDL is directly stored in the FIFO memory, sent to a computer and then the program eliminates a single element of TDL delay fluctuation errors.

Another source of error in the system is metastability. It is defined as:

$$MTBF(t_r) = \frac{\exp\left(\frac{t_r}{\tau}\right)}{W \cdot f_c \cdot f_d}, \tag{5}$$

where: *MTBF* – Mean Time Between Failure, W, τ – parameters, f_c – signal frequency at a flip-flop clock input, f_d – signal frequency at a flip-flop data input, t_r – observation time.

Metastability is a random increase of the signal propagation. This is caused by a breach of time rules for reading and writing information in a single flip-flop. In the system, TDL registers are read after a minimum of *5 ns*. The estimated MTBF value is about 10^{14}, it means that the metastability does not have a significant impact on the result of measurement.

The last source of error in TIMM is reference clock signal stability [9]. At the beginning in the system an oscillator with the fifth overtone vibrations of a quartz crystal (EPSON F321G) is used as the reference clock. Undoubtedly, short-term and long-term stability affects significantly the result of time to digital conversion. The instability of such an oscillator as a function that measures the time interval is shown in Fig.7. Application of the oscillator limits the measurement range to a few microseconds. Increasing the range of a few microseconds to milliseconds will create larger errors in the time interval measurement. This inconvenience can be minimized by changing the reference signal source. The uncertainty of time interval measurement for the oscillator O 100.0-JOB75-3.3-1 is described in Fig. 8.

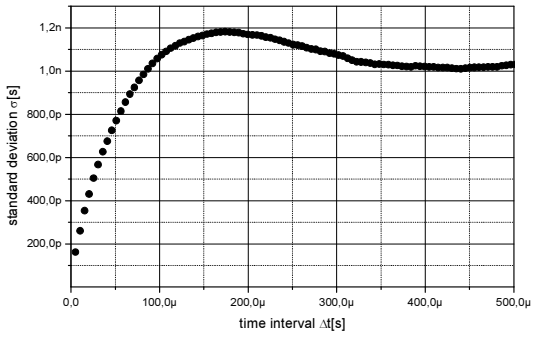

Fig. 7. Standard deviation as a function of time interval for reference clock EPSON F321G.

Metrol. Meas. Syst., Vol. XXI (2014), No. 1, pp. 77–84.

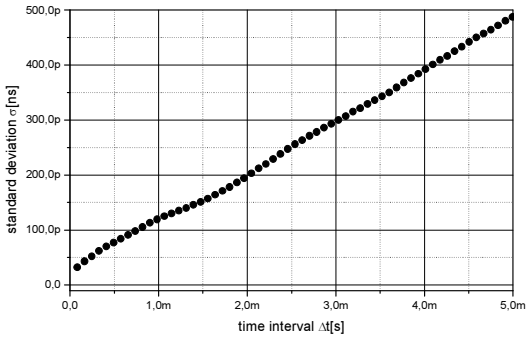

Fig. 8. Standard deviation as a function of time interval for reference clock O 100.0-JOB75-3.3-1.

Now the measuring range can be extended with the same uncertainty. When the influence of reference clock instability is minimized, the differential method of time measurement can be used (flow measurement application).

If all sources of errors are considered then the uncertainty of time interval measurement is reduced.

a) b)

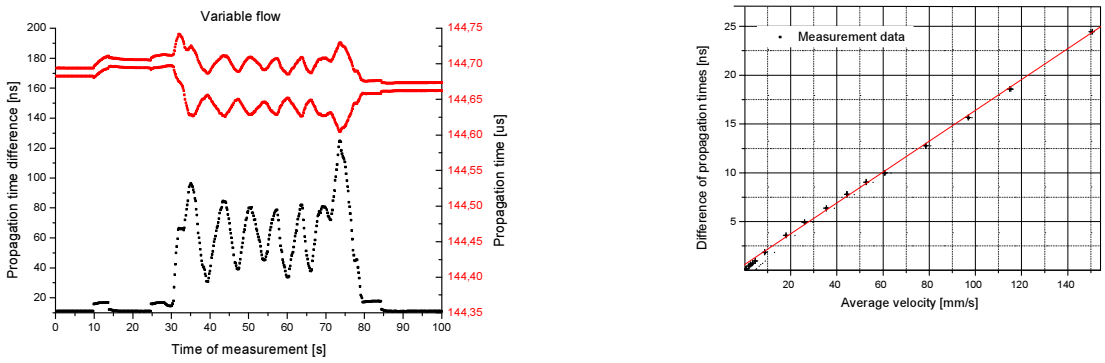

Fig. 9. Measurement data a) variable flow measurement, b) the flow measurement characteristics.

Because the FPGA structures are very flexible, there is a wide range of applications. One of them is flow measurement. The system presented in this article was just applied to flow measurement [10]. In this application some design changes were made. The first modification is to add the input circuit. So it is possible to use the differential method of time interval measurement. The second modification is the circuit in which excitation pulses to piezoelectric transducers are generated. These simple changes made it possible to use TIMM to flow measurement. As an example the variable flow measurement is shown (Fig. 9a). The system flow measurement characteristic was also made. The result of such investigation is presented in Fig. 9b.

5. Conclusions

The main problem of the high resolution time interval measurement systems implemented in a FPGA structure is designing the TDL. There are many solutions and one of them is the implementation of TDL in a carry chain. In the Virtex-5 device, it is possible to obtain an average resolution of about *15 ps.* As described in this article, there are few sources of error. One of them is theTIMM characteristics. Knowing this characteristics (nonlinearity), the result of measurement is improved. Another problem are the single element delay fluctuations. This error type is minimized when the hardware or software algorithm is used.

As described previously, the reference clock stability has also affected the result of measurement. The influence of this factor is minimized when the reference clock is changed or the method of measurement is changed. The FPGA package had a temperature of about 50 ^{o}C which was stable during the measurement process. The temperature of the other electronic devices was about 30 ^{o}C. Undoubtedly, the temperature fluctuations are a source of uncertainties. The influence of fluid temperature fluctuations is compensated by the flow measurement method where the flow is calculated based on the time interval measurement in two different directions. Of course, the voltage supply fluctuations will affect the system. Therefore in this device a voltage regulator was used.

The advantage of solutions presented in this article is the reduction of the uncertainty of time interval measurement when all sources of errors are considered. In this way, measurement of a flow of approximately 0.0008 m/s can be measured with small uncertainty.

Acknowledgments

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